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Shin Hung
Borden Ladner Gervais
World Exchange Plaza
1100-100 Queen Street
Ottawa, ON K1P 1J9
CANADA

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,873	KURJANOWICZ, WLODEK	
	Examiner	Art Unit	
	Ahmed Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 23-31* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/13/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed February 13, 2008 has been entered. Claims 2 and 15-22 have been cancelled and new claims 30 and 31 have been added.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 29 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The application as originally filed does not specifically support the claim limitation, "a field oxide adjacent to the fusible area". There is no discussion in the specification about a field oxide being adjacent to the fusible area.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated et al. ("Peng") US PG-Pub 2004/0156234.

Peng discloses (abstract and figs. 16 and 22-25) anti-fuse memory array comprising: a plurality of anti-fuse transistors arranged in rows and columns, each anti-fuse transistor including a polysilicon gate (par. 86) over a channel region in a substrate, the channel having a preset length; a diffusion region (see N+ implant adjacent the Normal/Thinner Gox shown in fig. 16) proximate to a first end of the channel region; a variable thickness gate oxide (Normal/Thinner Gox) between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion (Normal Gox) extending from the first end of the channel region to a predetermined distance of the preset length, and a thin gate oxide portion (Thinner Gox) extending from the predetermined distance to a second end of the channel region an oxide breakdown zone proximate to the second end of the channel region; bitlines **WL** coupled to the diffusion regions of a column of anti-fuse transistors; and, wordlines BL coupled to the polysilicon gates of a row of anti-fuse transistors.

6. Claims 23-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Peng.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: an active channel area; a polysilicon gate (par. 86) formed over the active channel area to define a fusible edge (adjacent Thinner Gox) to and an access edge (adjacent Normal Gox); a thick gate oxide (Normal Gox) adjacent to the access edge; a first diffusion region adjacent to the access edge; a second diffusion region adjacent to the fusible edge (see N+ implant adjacent the Normal/Thinner Gox shown in fig. 16); and a thin gate oxide (Thinner Gox) over the active channel area adjacent to the fusible edge, the thin gate oxide having a lower

breakdown voltage than the thick gate oxide for forming a conductive link between the polysilicon gate and the active channel area.

Re claim 24, a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 25, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Re claim 26, Peng discloses the polysilicon gate defines the active channel area between the fusible edge and the access edge, and the thick gate oxide and the thin gate oxide are disposed between the channel region and the polysilicon gate, the thick gate oxide extending from the access edge to a predetermined length of the active channel area, and the thin gate oxide extending from the predetermined length of the active channel area to the fusible edge.

The recitation of claim 27 calling for, "the thick gate oxide portion includes a combination of an intermediate gate oxide and the thin gate oxide portion" fails to further limit the anti-fuse structure.

Re claim 28, Peng discloses the polysilicon gate (par. 86) has a first portion disposed over the thick gate oxide (Normal Gox) and located adjacent to the diffusion region for defining the active channel area, the access edge being defined by a first portion edge, and a second portion disposed over the thin gate oxide (Thinner Gox) and coupled to the first portion, the fusible edge being defined by a second portion edge, the second diffusion region being disposed between the fusible edge and the active channel area.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 and 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peng in view of Hush et al. ("Hush") USPN 7,002,833.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: a polysilicon gate (par. 86) over a channel region in a substrate, the channel having a preset length; a diffusion region (see N+ implant adjacent the Normal Gox shown in fig. 16) proximate to a first end of the channel region (figs. 16, 22 and 23); an isolation region (see N+ implant adjacent the Thinner Gox shown in fig. 16) proximate to a second end of

the channel region; a variable thickness gate oxide (Normal and Thinner Gox) between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion (Normal Gox) extending from the **first end** of the channel region to a predetermined distance of the preset length, a thin gate oxide portion (Thinner Gox) extending from the predetermined distance to the **second end** of the channel region (figs. 16, 22 and 23), but does not specifically disclose a field oxide.

Hush discloses in fig. 1 a field oxide region proximate to an end of a channel region.

Therefore, in view of Hush's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Peng by incorporating a field oxide proximate a channel region. The motivation would be to provide a memory cell isolation. Therefore, it would have been obvious to combine Peng with Hush to yield the device of claim 1.

Regarding the recitation calling for, "a breakdown resistant access edge proximate to the **first end** of the channel region for conducting current between the polysilicon gate and the diffusion region; and an oxide breakdown zone proximate to the **second end** of the channel region, the oxide breakdown zone fusible to form a conductive link between the polysilicon gate and the channel region," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his

claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 3, Peng discloses (par. 91) a thin gate oxide portion corresponding to a gate oxide of a low voltage transistor formed on the semiconductor material.

Re claim 4, Peng discloses (paragraphs 8 and 10) a thick gate oxide portion is identical to at least one high voltage transistor gate oxide formed on the semiconductor material.

The recitation of claim 5 calling for, "the thick gate oxide portion includes a combination of an intermediate gate oxide and the thin gate oxide portion" fails to further limit the anti-fuse structure.

Re the recitation of claim 6 calling for, "the floating diffusion region, the second end of the channel region and a gate edge of the polysilicon gate have a common edge defined by at least two line segments being at an angle to each other," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re the recitation of claim 7 calling for, "angle is one of 135 degrees and 90 degrees," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252,

1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 8, Peng discloses the diffusion region has an LDD implant (fig. 22) identical to the LDD implant of the low voltage transistor/the high voltage transistor (paragraphs 8, 10 and 91) which is one of the low voltage transistor, the high voltage transistor and a combination of both the low and the high voltage transistors.

Re claim 9, Peng discloses an edge of the diffusion region and a portion of the polysilicon gate is free of salicidation.

9. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peng in view of Oyama ("Oyama") JP 4-44273.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: an active channel area (unnumbered); a polysilicon gate (par. 86) formed over the active channel area to define a fusible area (adjacent Thinner Gox), an access edge (adjacent Normal Gox); a thick gate oxide (Normal Gox) adjacent to the access edge; a diffusion region (N+ implant) adjacent to the access edge; and a thin gate oxide (Thinner Gox) having the fusible area between the thick gate oxide and the isolation edge, but does not disclose a field oxide adjacent to the fusible area.

Oyama discloses in fig. 1 a field oxide 4 adjacent to a fusible area.

Therefore, in view of Oyama's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Peng by incorporating a field oxide. The motivation would be to provide a memory cell isolation. Therefore, it would have been obvious to combine Peng with Oyama to yield the device of claim 29.

10. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peng in view of Oyama.

Peng discloses in figs. 16 and 22-25 an anti-fuse transistor formed on a semiconductor material comprising: a polysilicon gate (par. 86) over a channel region in a substrate, the channel having a preset length; a diffusion region (see N+ implant adjacent the Normal Gox shown in fig. 16) proximate to a first end of the channel region (figs. 16, 22 and 23); an isolation region (see N+ implant adjacent the Thinner Gox shown in fig. 16) proximate to a second end of the channel region; a variable thickness gate oxide (Normal and Thinner Gox) between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion (Normal Gox) extending from the **first end** of the channel region to a predetermined distance of the preset length, a thin gate oxide portion (Thinner Gox) extending from the predetermined distance to the **second end** of the channel region (figs. 16, 22 and 23), but does not specifically disclose an isolation region.

Oyama discloses in fig. 1 an isolation region 4 proximate to a channel region.

Therefore, in view of Oyama's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Peng by incorporating a field oxide. The motivation would be to provide a memory cell isolation. Therefore, it would have been obvious to combine Peng with Oyama to yield the device of claim 30.

Regarding the recitation calling for, "a breakdown resistant access edge proximate to the **first end** of the channel region for conducting current between the polysilicon gate and the diffusion region; and an oxide breakdown zone proximate to the **second end** of the channel region, the oxide breakdown zone fusible to form a conductive link between the polysilicon gate and the channel region," a prima facie case of anticipation has been established because the claimed and prior art products are identical or substantially identical in structure and/or composition. *In re Best,* 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product."). *See also In re Spada,* 911 F.2d 705, 708-09, 15 USPQ2d 1655, 1657-58 (Fed. Cir. 1990).

Re claim 31, Oyama discloses in fig. 1 a field oxide proximate to a thin oxide portion 2'.

Allowable Subject Matter

11. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments filed 2/13/08 have been fully considered but they are not persuasive.

Contrary to Applicant's assertion that Peng does not teach a thin oxide portion corresponding to a low voltage transistor, Peng discloses that that is the case in most cases which implies that in few cases a thin oxide portion would correspond to a low voltage transistor.

Note that Applicant did not argue regarding the rejections of independent claims 10 and 23, therefore, the rejection of claims 10 and 23 are being maintained.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. Sefer/
Primary Examiner
Art Unit 2826